**EXPEDITED PROCEDURE – EXAMINING GROUP 2816**

S/N 10/750,320 **PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicant: | Edward A. Burton et al. | Examiner: Anh-Quan Tra |
| Serial No.: | 10/750,320 | Group Art Unit: 2816 |
| Filed: | December 31, 2003 | Docket No.: 884.C02US1 |
| Title: | APPARATUS AND METHOD TO CONTROL SELF-TIMED AND SYNCHRONOUS SYSTEMS | |
| Assignee: | Intel Corporation | Customer Number: 21186 |

## PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Final Office Action mailed September 22, 2005, the Applicant requests review of the final rejection in the above-identified Application. No amendments are submitted with this Request, which is being filed with a Notice of Appeal for the reasons stated below.

### §102 Rejection of the Claims

Claims 1-2, 6-18, 26-27, and 29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mizuno et al. (U.S. 6,166,577). Applicant believes there is a clear deficiency in the *prima facie* case in support of the rejection, namely, that the Final Office Action has not shown that Mizuno et al. discloses the identical invention as claimed.

Anticipation under 35 U.S.C. § 102 requires the disclosure in a single prior art reference of each element of the claim under consideration. *See Verdegaal Bros. V. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis

added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

Applicant's previous response (mailed August 12, 2005, hereinafter the "Previous Response") to the Non-final Office Action mailed on June 14, 2005 in this matter on page 8 states,

> Claims 1 and 12 recite, "a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current." Claim16 recites, "a leakage timing circuit formed on the substrate, the leakage timing circuit having a leakage current and the leakage timing circuit to generate a signal having a frequency related to the leakage current." Claim 26 recites, "generating a second signal related to a leakage current."

Further, the Previous Response on page 9 states,

> Applicant respectfully submits that the Office Action fails to produced any evidence to show that the elements of a leakage timing circuit having a frequency related to a leakage current (as recited in claims 1, 12, and 16) and generating a second signal related to a leakage current (as recited in claim 26) are necessarily present in Mizuno et al. Thus, the Office Action fails to show in a single reference, either explicitly or inherently, all of the elements recited in claims 1, 12, 16, and 26.

In response to these arguments, the Final Office Action on page 6 relies on Mazakaki et al. (USP 6489833) and Teraoka et al. (USP 6333571) to support the statement, "The above examples demonstrate that it is inherent that substrate bias voltage determines the leakage current of transistor." While Applicant does not necessarily agree with the statement, even if true, the statement still fails to show how any of these references teach, for example, "a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current," as recited in claim 1. Further, the Final Office Action fails to show how any of these references teach, for example, "generating a signal related to a leakage current," as recited in claim 26. Because Mizuno et al. fails to show in a single prior reference a disclosure of each and every element of the claimed invention, arranged as in at least claims 1, 12, 16, and 26, the

Final Office Action fails to state a *prima facie* case of anticipation with respect to claims 1-2, 6-18, 26-27, and 29.

## §103 Rejection of the Claims

*Claims 3-5 and 19-20*

Claims 3-5 and 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. (U.S. 6,166,577) in view of Klemmer (U.S. 6,337,601). Applicant respectfully maintains the traversal of the rejection of claims 3-5 and 19-20.

As stated on pages 10-11 of the Previous Response, claims 3-5 depend from claim 1, and claims 19-20 depend from claim 16. Applicant believes they established in the Previous Response that the proposed combination of Mizuno et al. with Klemmer fails to teach or suggest all of the elements of claims 3-5 and 19-20.

In addition, Applicant maintains the arguments on pages 10-11 of the Previous Response with respect to additional elements missing from the cited references and included, for example, in claim 5. As noted in the Previous Response, the proposed combination of Mizuno et al. and Klemmer fails to teach or suggest, "wherein the frequency related to the leakage current is substantially proportion to the leakage current," as recited in claim 5. In response to that argument, the Final Office Action on page 6 states, "Such characteristic is inherent in Mizuno et al.'s circuit because the threshold of the transistor is related to the leakage current of the transistor, and the speed of the transistor is related to the threshold of the transistor." (Emphasis added).

Applicant disagrees. And while Applicant does not admit that this statement is true, the statement still fails to show how the proposed combination of references teaches or suggests a frequency related to the leakage current. Applicant also submits that the "speed of a transistor" fails to teach or suggest a frequency related to the leakage current substantially proportional to the leakage current, as recited in claim 5. Thus, Applicant maintains that the Final Office Action fails to provide any evidence to show that frequency is related to the leakage current, or that such a characteristic is inherent in Mizuno et al. because of the statement that the threshold

of the transistor is related to the leakage current of the transistor, and the speed of the transistor is related to the threshold of the transistor.

In addition, Applicant maintains the arguments presented on page 11-12 of the Previous Response with regards to the previous Office Action's failing to provide a proper basis for forming the proposed combination of Mizuno et al. with Klemmer. In response to these arguments, the Final Office Action on page 6 states, "One skilled in the art would have been motivated to add a frequency divider (counter) to Mizuno et al.'s circuit in order to increase the OSC's frequency N time the CLK1's frequency." Applicant disagrees. Further, the statement is not supported by the cited references, and still further, as noted in the Previous Response, the statement destroys the stated purpose in Mizuno of locking the frequency of the OSC1 oscillator to the frequency of output CLK1.

For at least these reasons and the reasons stated in the Previous Response, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 3-5 and 19-20.

*Claims 28 and 30*

Claims 28 and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. (U.S. 6,166,577). Applicant respectfully maintains the traversal of the rejection of claims 28 and 30.

With respect to claims 28 and 30, Applicant maintains the arguments presented on pages 12-13 of the Previous Response, including Applicant's traversal of the taking of official notice with respect to these claims. In response to these arguments, the Final Office Action on page 7 refers to USP 6067612 figure 2, and USP 6044937 figure 1. However, the Final Office Action fails to point out where these references teach or suggest the elements as recited in claims 28 and 30. Further, the Final Office Action fails to provide any teaching of a motivation or suggestion to combine these references with the references used in making the rejection of claims 28 and 30. Still further, the Final Office Action, like the previous Office Action, fails to show how "it would have been obvious to one having ordinary skill in the art to use Mizuno et al. in communication

circuit for the purpose of saving power consumption," as recited on page 7 of the Final Office Action.

For at least these reasons and the reasons stated in the Previous Response, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 28 and 30.

*Conclusion*

For at least the reasons stated above and in Applicant's Previous Response of August 12, 2005, it is believed that the pending claims should be allowed. Reconsideration and withdrawal of the rejections under §§ 102 and 103 as a result of this Pre-Appeal Brief Request for Review is respectfully requested. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

Edward A. Burton et al.

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Date JAN. 23/2006

By Robert Madden
Robert Madden
Reg. No. 57,521

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 23rd day of January 2006.

Amy Moriarty

Name

Signature